IN THE CLAIMS

Please amend the claims as follows:

Claims 1-14 (Canceled).

Claim 15 (Original) An image processing circuit of an image input device which performs a predetermined image processing of image photographed by an image pickup device in said image input device, said circuit comprising:

a real time processing unit in which a predetermined general image processing of a pixel data being photographed by said image pickup device and inputted sequentially is performed by real time processing; and

a main memory that stores a pixel data outputted from at least said real time processing unit, in image frame units, and wherein,

said real time processing unit further comprises a defective pixel compensation block that reads defective pixel addresses stored in said main memory disposed outside of said real time processing unit, and performs defective pixel compensation when a pixel address of a pixel data residing in image matches said defective pixel address.

Claim 16 (Original) The image processing circuit according to claim 15 wherein, when a plurality of defective pixel addresses are present in said main memory, said defective pixel addresses are stored in the order of a pixel array sequence;

said defective pixel compensation block of said real processing unit comprises: a shift register with a plurality of registers connected in series, to which defective pixel addresses stored in said main memory are inputted sequentially; and

a comparator connected to the rearmost stage of said shift register in which an address count value of a pixel data inputted sequentially is compared with a defective pixel address provided from the said rearmost stage and, when a match is found, a defective pixel timing signal is outputted, characterized in that:

said shift register holds a defective pixel address, and output of the said rearmost stage is looped to an input terminal of the foremost stage;

said comparator is a comparator in which an address count value of a pixel data inputted sequentially is compared with a defective pixel address provided from the said rearmost stage and, when a match is found, a shift timing signal and a defective pixel timing signal are outputted; and

shift of said shift register is executed by said shift timing signal provided from said comparator.

Claims 17-27 (Canceled).